

Program Status Word (PSW) in Microcontroller 8051

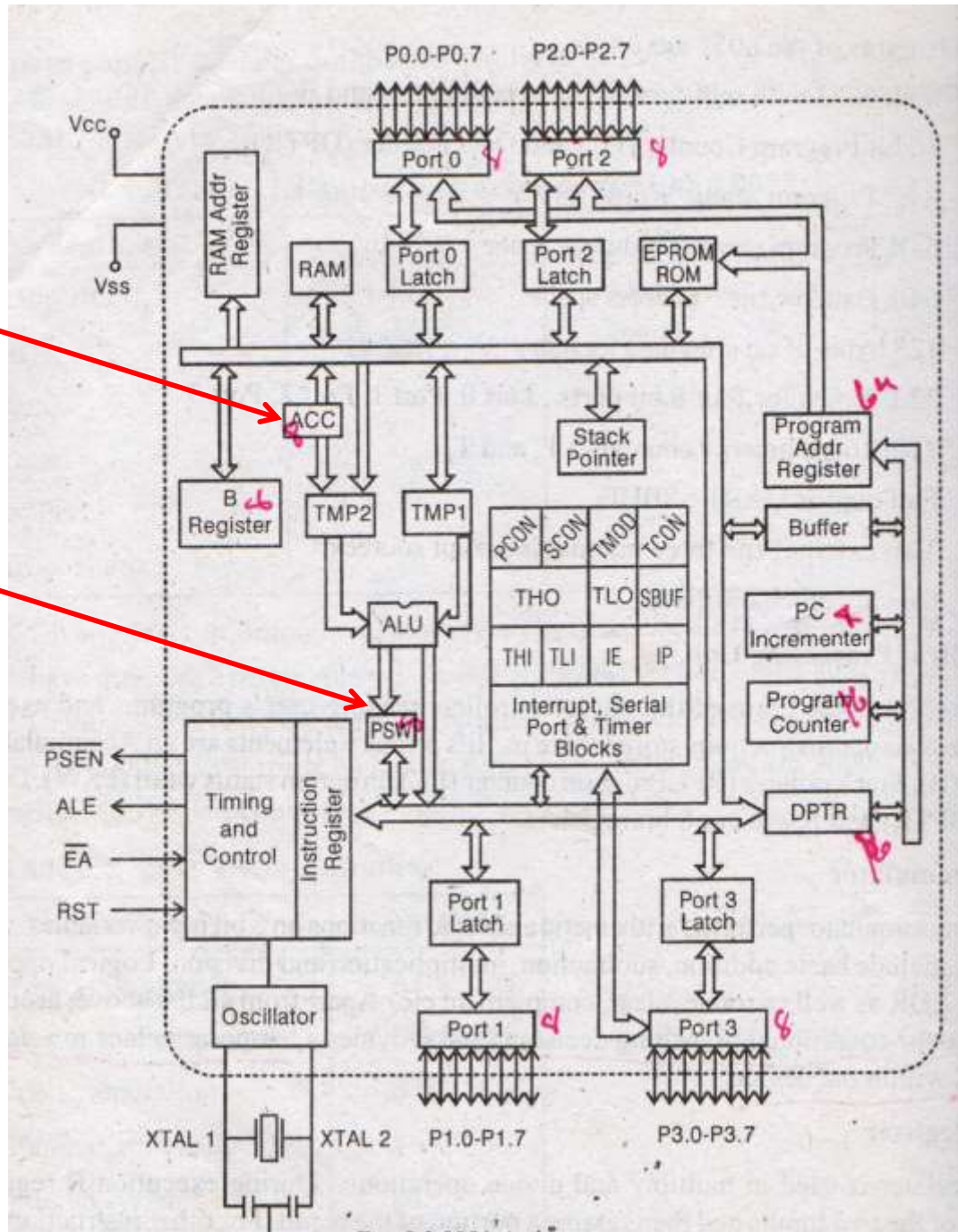


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Architecture of Intel 8051

Register A

Program Status Word (PSW)



128 byte Internal RAM

Memory Bank Select bits in PSW

11	7FH	Scratch Pad	
	30H		
10	2FH	Bit addressable (00-7F)	
	20H		
01	1FH	Bank 3	R7
	18H		R0
00	17H	Bank 2	R7
	10H		R0
01	0FH	Bank 1	R7
	08H		R0
00	07H	Bank 0	R7
	00H		R0

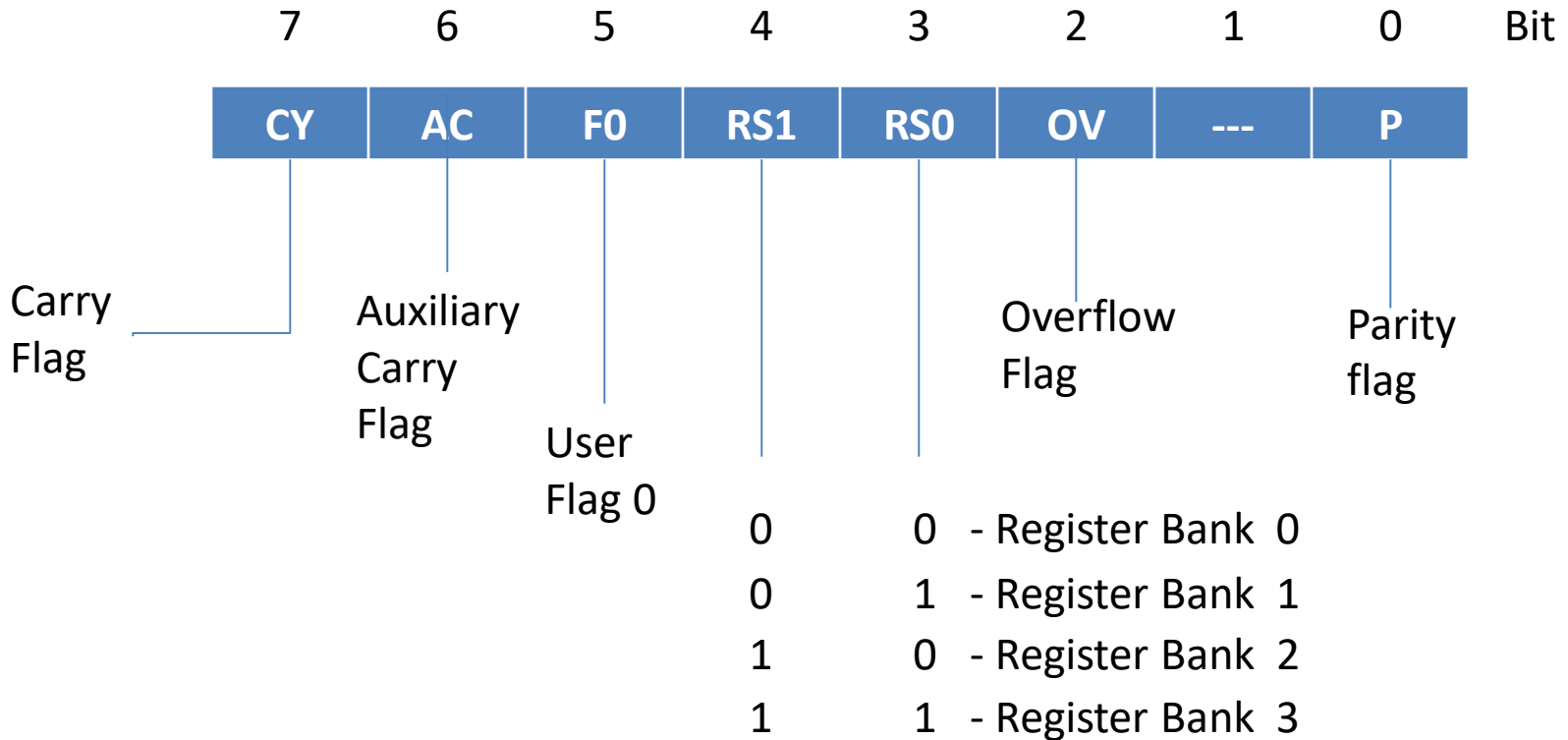
Bit Addressable Space

2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00

← Reset value of Stack Pointer

Intel 8051

Program Status Word (PSW 8-bit)



- Four math flags that respond automatically to the outcomes of the math operations
- Three general purpose user flags that can be set to 1 or cleared to 0 by the programmer



AC(Auxiliary Carry flag):

- Set to 1 when ever there is a carry from D3 to D4 during ADD or SUB operation
- This flag is used by instruction that perform BCD (binary coded decimal) arithmetic

CY (carry flag):

- Set to 1 whenever there is a carry out from the D7 bit
- Affected after 8 bit addition or subtraction
- Set to 1 or clear to 0 directly by an instruction such as " SET B C" and "CLR C"



P (parity flag):

- The parity flag reflect the number of 1's in the Reg. A only
- if the Reg. A contains an odd number of 1's then P=1
if Reg. A has even number of 1's the P=0

Reg. A

4AH = 0100 1010 P = 1

5AH = 0101 1010 P = 0

PSW



OV (overflow flag):

- This flag is set whenever the result of a signed number operation is too large causing the high order bit to overflow into the sign bit range (-128 to 127)
- the OV flag is only used to detect error in signed arithmetic operations.

Unsigned binary addition

PSW .	7	6	5	4	3	2	1	0	
	CY	AC	FO	RS1	RS0	OV	---	P	
	1	1	0	1	0	0	0	1	= D1H

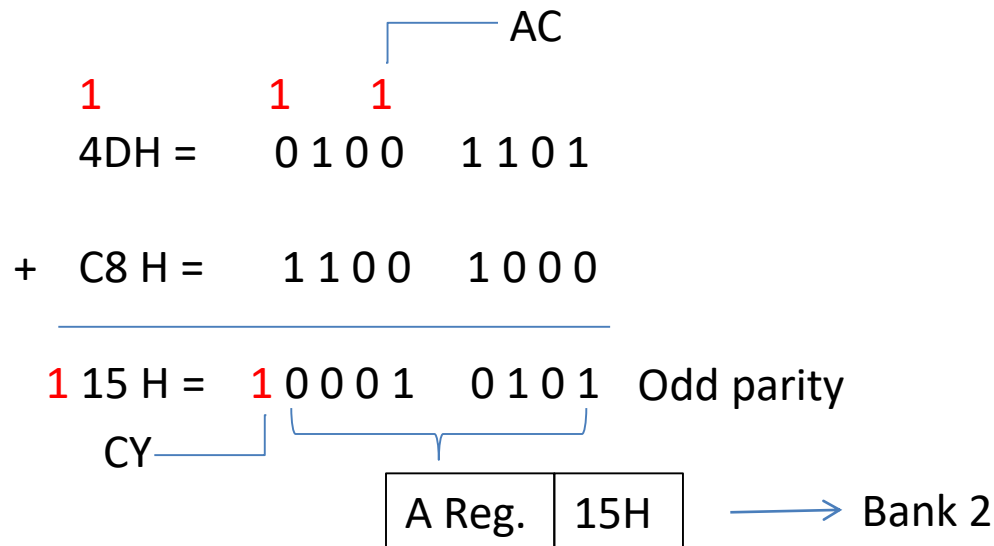
MOV A, #4DH ; move the data 4D into accumulator (A= 4DH)

MOV B, #C8H ; move the data C8 into B reg. (B=C8H)

ADD A,B ; add the content of B reg. with A reg. (A=15H)

SETB PSW.4 ; select bank 2

MOV R0, A ; move 15H data from accumulator to R0 (Ram location 10H)



Signed binary numbers

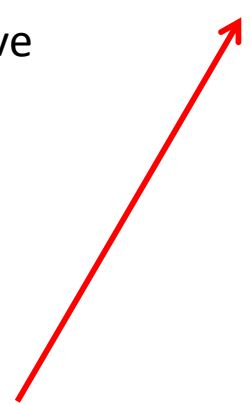


D7 (MSB) is the sign and D0 to D6 are the magnitude of the number

- If D7=0, the operand is +ve, and if D7=1, it is -ve
- Positive numbers are 0 to +127
- Negative numbers are -1 to -128
- 2's complement represents negative number

$$\begin{array}{r}
 (+1)_{10} = 0000\ 0001 \\
 \underline{1111\ 1110} \\
 1 \\
 \hline
 1111\ 1111 = (-1)_{10}
 \end{array}$$

Decimal	Binary	Hex
-128	1000 0000	80
-127	1000 0001	81
-126	1000 0010	82
...
-2	1111 1110	FE
-1	1111 1111	FF
0	0000 0000	00
+1	0000 0001	01
+2	0000 0010	02
...
+127	0111 1111	7F



When Over Flow Fag (OV) is set?

MOV A, # -128 ; A = 1000 0000 (80H)

MOV R1, # -2 ; R1 = 1111 1110 (FEH)

ADD A, R1 ; A = 0111 1110
; (A= 7E = -130, Invalid)

	-128	1	0	0	0	0	0	0	0
(+)	-2	1	1	1	1	1	1	1	0

-130 1 0 1 1 1 1 1 1 0

OV= 1

When Over Flow Fag (OV) is set?

MOV A, # -5 ; A = 1111 1011 (FBH)

MOV R1, # -2 ; R1 = 1111 1110 (FEH)

ADD A, R1 ; A = 1111 1001
; (A= F9 = -7 , valid)

		1	1	1	1	1	1		
	-5	1	1	1	1	1	0	1	1
(+)	-2	1	1	1	1	1	1	1	0

	-7	1	1	1	1	1	0	0	1

OV= 0

When Over Flow Fag (OV) is set?

MOV A, # -2 ; A = 1111 1110 (FEH)

MOV R1, #-128 ; R1 = 1000 0000 (80H)

SUBB A, R1 ; A = 0111 1110
; (A= 7E = +126 , valid)

	-2	1	1	1	1	1	1	1	0
(-)	-128	1	0	0	0	0	0	0	0

126	0	1	1	1	1	1	1	0
-----	---	---	---	---	---	---	---	---

OV= 0

When Over Flow Flag (OV) is set?

MOV A, # -50 ; A = 1100 1110 (CEH)

MOV R1, #+100 ; R1 = 0110 0100 (64H)

SUBB A, R1 ; A = 0110 1010
; (A= 6A = -150, Invalid)

-50	1	1	0	0	1	1	1	0
(-) +100	0	1	1	0	0	1	0	0
		1	1					

-150	0	1	1	0	1	0	1	0
------	---	---	---	---	---	---	---	---

OV= 1

DIVISION :

$$\begin{array}{r} A \\ \hline B \end{array}$$

If $B = 0$, $OV = 1$ indicates error

If $B \neq 0$, $OV = 0$

- `JB PSW.2` ; Jump if direct bit is set
- `JNB PSW.2` ; Jump if direct bit is not set

Special Function Registers (SFRs)

Register Name	Function	Address (Hex)
Acc (A)	Accumulator	E0
B	Arithmetic	F0
DPH	Data Pointer High byte	83
DPL	Data Pointer Low byte	82
IE	Interrupt Enable control	A8
IP	Interrupt Priority control	B8
P0	I/O Port 0 Latch	80
P1	I/O Port 1 Latch	90
P2	I/O Port 2 Latch	A0
P3	I/O Port 3 Latch	B0
PCON	Power Control	87

Special Function Registers (SFRs)

Register Name	Function	Address (Hex)
PSW	Program Status Word	D0
SCON	Serial Port Control	98
SBUF	Serial Port Data Buffer	99
SP	Stack Pointer	81
TMOD	Timer/ Counter Mode control	89
TCON	Timer/Counter Control	88
TL0	Timer 0 low byte	8A
TH0	Timer 0 high byte	8B
TL1	Timer 1 low byte	8C
TH1	Timer 1 high byte	8D

Special Function Registers (SFRs)

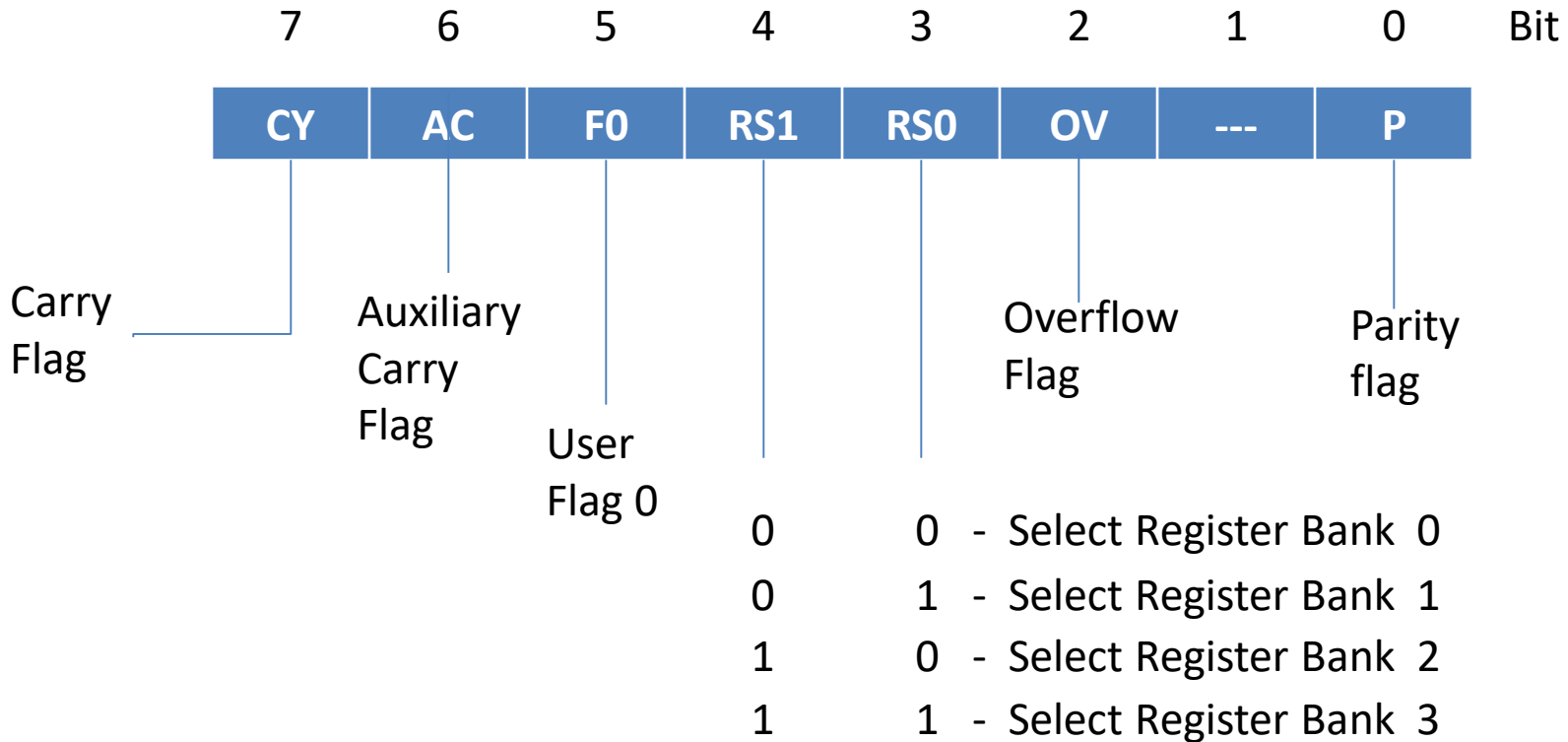
SFR RAM Address (Byte and Bit)

Byte address	Bit address		Byte address	Bit address	
FF			98	9F 9E 9D 9C 9B 9A 99 98	SCON
F0	F7 F6 F5 F4 F3 F2 F1 F0	B	90	97 96 95 94 93 92 91 90	P1
E0	E7 E6 E5 E4 E3 E2 E1 E0	ACC	8D	not bit addressable	TH1
D0	D7 D6 D5 D4 D3 D2 D1 D0	PSW	8C	not bit addressable	TH0
			8B	not bit addressable	TL1
B8	-- -- -- BC BB BA B9 B8	IP	8A	not bit addressable	TL0
			89	not bit addressable	TMOD
B0	B7 B6 B5 B4 B3 B2 B1 B0	P3	88	8F 8E 8D 8C 8B 8A 89 88	TCON
			87	not bit addressable	PCON
A8	AF AE AD AC AB AA A9 A8	IE			
			83	not bit addressable	DPH
A0	A7 A6 A5 A4 A3 A2 A1 A0	P2	82	not bit addressable	DPL
			81	not bit addressable	SP
99	not bit addressable	SBUF	80	87 86 85 84 83 82 81 80	P0

Thank You

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